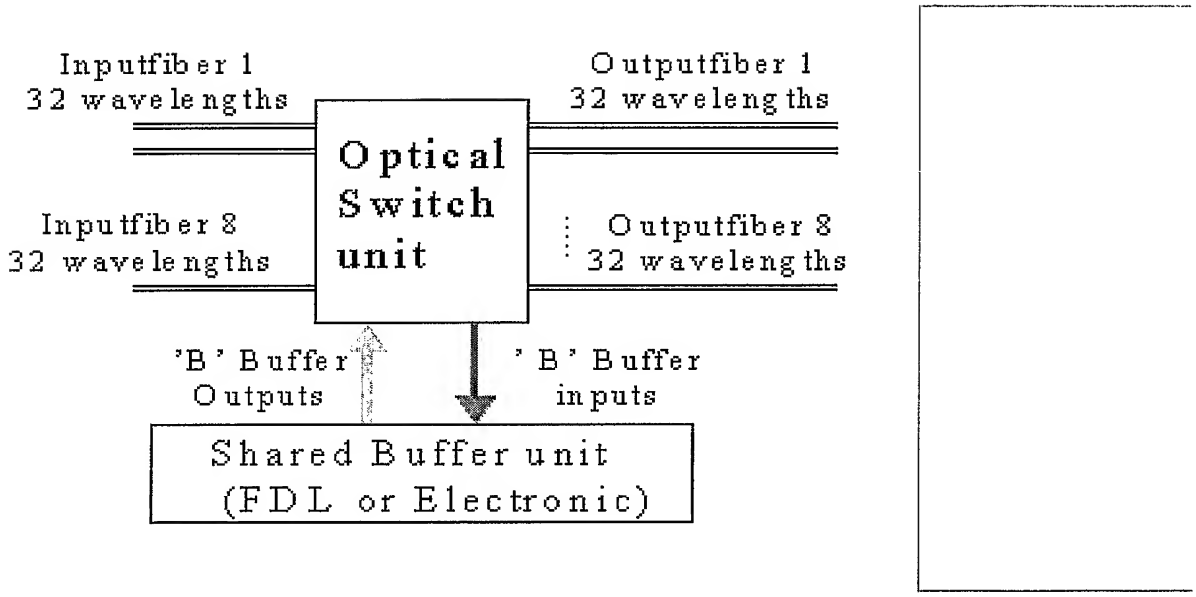

Fig. 1. Generic model of simulated switch.

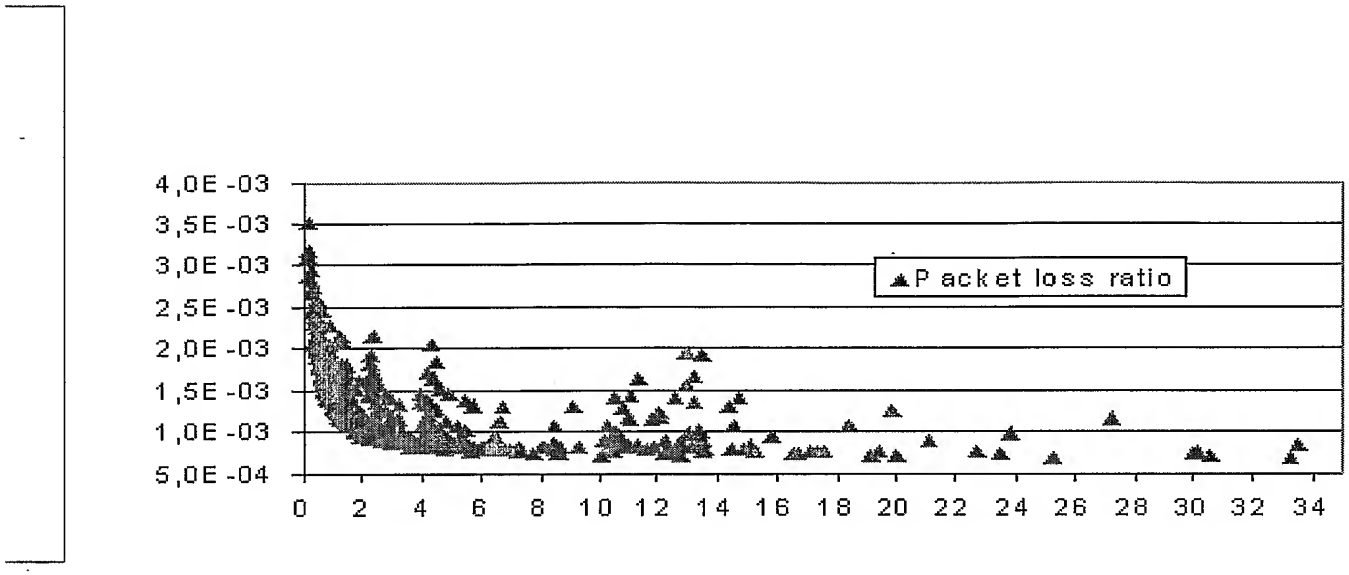

Figure 2. PLR (Y-axis) as a function of time packets stay in the buffer (X-axis). Clocking in and out of the buffer is not counted into the delay. Some of the plotted points, indicates both high PLR and delay. These points are a result of unfavorable combinations of Wv_1-Wv_3.

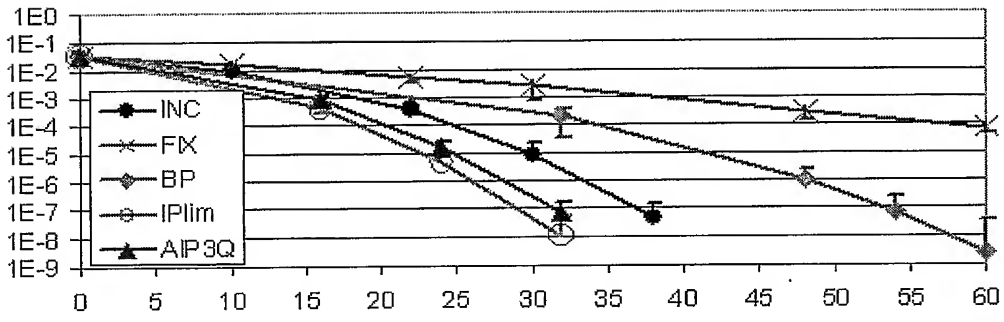

Figure 3. PLR (Y-axis) as a function of number of buffer interfaces (X-axis).

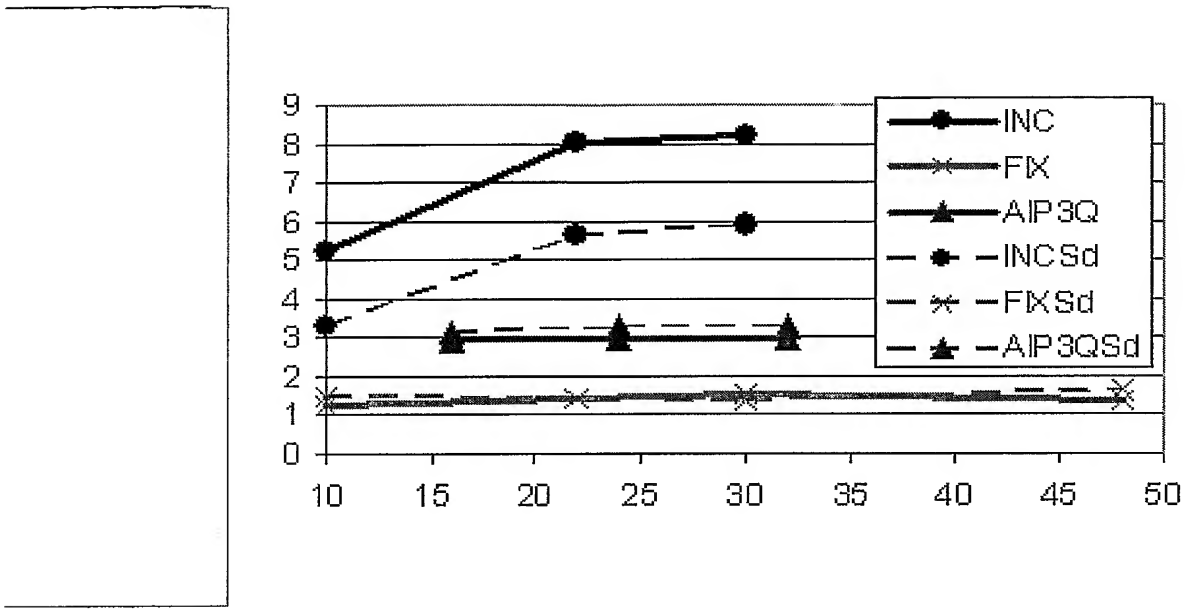

Figure 4. Delay in units of duration of mean packet length (units, Y-axis), as a function of number of buffer interfaces (X-axis).
Sd = Standard Deviation